

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. **(Currently Amended)** A memory cell, comprising:

a first node for storing a first potential;

a second node for storing a second potential;

transistor gate electrodes formed from a gate layer; and

a capacitor having plates coupled between the first node and second node, a portion of one plate of the capacitor comprising a first

interconnect wiring ~~layer~~ pattern, ~~formed over the gate layer~~, that

includes a plurality of conductive layers ~~and that electrically interconnects circuit devices of the memory cell~~ commonly etched into the same pattern with substantially aligned edges.

2. (Original) The memory cell of claim 1, further comprising:

a first inverter having an input coupled to the first node and an output coupled to the second node; and

a second inverter having an input coupled to the second node and an output coupled to the first node; wherein

the first node stores a true data value and the second node stores a complementary data value.

3. (Original) The memory cell of claim 1, further including:

a first access transistor coupled to the first node; and

a second access transistor coupled to the second node.

4. (Cancelled)

5. **(Currently Amended)** The memory cell of claim 1, wherein:

the first interconnect wiring ~~layer~~ pattern includes a plurality of separate portions, each portion including bottom conductive layer, ~~at the~~ dielectric layer formed over the bottom conductive layer, and a top conductive layer formed over the dielectric layer, the bottom conductive

layer forming at least a portion of a first plate of the capacitor, the bottom conductive layer, dielectric layer, and top conductive layer having the same pattern.

- 5     **6. (Currently Amended)** The memory cell of claim 5, further including:  
          a second conductive interconnect wiring formed over the first  
interconnect wiring ~~layer~~-pattern that forms at least a portion of a second  
plate of the capacitor.

7. (Previously Presented) The memory cell of claim 6, wherein:  
10           the second conductive interconnect wiring comprises titanium;  
          the bottom conductive layer comprises titanium nitride; and  
          the top conductive layer comprises titanium.

Claims 8 to 20 (Cancelled)

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21. (Previously Presented) The memory cell of claim 1, wherein:  
          the gate layer is not in physical contact with a drain of any  
transistor of the memory cell.

- 20     **22. (Currently Amended)** The memory cell of claim 1, wherein:

~~a first interconnect wiring that includes~~ the first interconnect  
wiring ~~layer~~-pattern, includes

- a first portion of the first interconnect wiring ~~is in physical contact~~  
~~with the~~ comprising a bottom conductive layer formed below a  
25     dielectric layer that isolates the bottom conductive layer from a top  
conductive layer, the bottom conductive layer electrically connecting  
drains of a first and second transistor of the memory cell; ~~and~~

- ~~a second portion of the first interconnect wiring, separate from~~  
~~the first portion, is in physical contact with the drains of a third and~~  
30     ~~fourth transistor of the memory cell.~~

23. (Currently Amended) A memory cell, comprising:

a first data storage node;

a second data storage node; ~~and~~

a capacitor comprising a first plate coupled to the first data storage  
5 node, a second plate coupled to the second data storage node, and a  
third plate separated from the first and second plates by a capacitor  
dielectric, ~~the first and second plates comprising portions of an  
interconnect layer that electrically connects terminals of transistors  
of the memory cell to one another; and~~

10 a plurality of wiring portions, each comprising a commonly  
patterned first conductive layer and dielectric layer, a first wiring  
portion forming the first plate and a second wiring portion forming  
the second plate, the dielectric layer forming the capacitor dielectric.